WHAT IS CLAIMED IS:

1. An image signal processing apparatus comprising:

a first resizing circuit for resizing input image data;

a first memory for storing the image data output from said first resizing circuit;

a second memory for temporarily storing the image data read from said first memory and being able to asynchronously perform data writing and data reading;

a processing circuit for performing a predetermined process to the image data read from said second memory; and

a P/S (parallel-to-serial) conversion circuit for converting the image data from said processing circuit into serial signals of which the number is smaller than the number of bits of the image data from said processing circuit.

2. An apparatus according to Claim 1, wherein said processing circuit includes a conversion circuit for converting the image data read from said second memory into image data of RGB format.

3. An apparatus according to Claim 2, wherein said processing circuit includes a dot sequential conversion circuit for converting the image data of RGB

format into a dot sequential signal.

4. An apparatus according to Claim 3, wherein said processing circuit includes a sync signal addition circuit for adding a sync signal to dot sequential R, G and B signals.

5. An apparatus according to Claim 4, further comprising:

an image display unit for performing image display on the basis of the serial data output from said P/S conversion circuit; and

a display control circuit for performing a process to display on said image display unit the serial data output from said P/S conversion circuit corresponding to said image display unit.

6. An apparatus according to Claim 1, wherein the input image data is composed of a brightness component and a color difference component.

7. An apparatus according to Claim 1, wherein said processing circuit includes

a second resizing circuit for resizing the image data read from said second memory more smaller,

a first signal processing circuit for performing a predetermined signal process to the image data read

from said second resizing circuit, and

a second signal processing circuit for performing a predetermined signal process to the image data sent without said second resizing circuit.

8. An apparatus according to Claim 7, wherein said processing circuit includes a conversion circuit for converting the image data read from said second resizing circuit into image data of RGB format.

9. An apparatus according to Claim 7, further comprising:

a D/A (digital-to-analog) conversion circuit for performing D/A conversion to the image data processing by said second signal processing circuit;

a band limiting circuit for band-limiting to the analog image signal from said D/A conversion circuit;

an amplifier for amplifying the output from said band limiting circuit; and

an output unit for outputting the analog image signal from said amplifier.

10. An apparatus according to Claim 7, wherein the input image data is composed of a brightness component and a color difference component.

11. An apparatus according to Claim 7, wherein

said second signal processing circuit converts the image data read from said second memory into image data of composite format.

12. An apparatus according to Claim 1, wherein said processing circuit includes

a conversion circuit for converting the image data read from said second memory into image data of composite format, and

a sync signal addition circuit for adding a sync signal to a composite signal output from said conversion circuit.

13. An apparatus according to Claim 1, wherein a storage capacity of said second memory is smaller than a storage capacity of said first memory.

14. An apparatus according to Claim 5, wherein said dot sequential conversion circuit changes an RGB output dot sequential string among previously set RGB dot sequential strings, corresponding to an RGB dot sequential string of said image display unit.

15. An apparatus according to Claim 5, wherein a resizing rate of said first resizing circuit is changed corresponding to a display pixel size of said image display unit.

16. An image signal processing apparatus comprising:

a first resizing circuit for resizing input image data;

a first memory for storing the image data output from said first resizing circuit;

a second memory for temporarily storing the image data read from said first memory and being able to asynchronously perform data writing and data reading;

a TV signal processing circuit for performing a predetermined signal process to the image data read from said second memory to generate a TV image signal;

an LPF (low-pass filter) for performing an LPF process to the image data read from said second memory; and

a data conversion circuit for converting the image data from said LPF into image data of predetermined image display format.

17. An apparatus according to Claim 16, wherein an oscillation clock of said TV signal processing circuit is 14.31818MHz, a horizontal size of the image data output from said first resizing circuit is 752 pixels, and the number of horizontal pixels in the predetermined image display format is less than 752 pixels.

18. An apparatus according to Claim 16, wherein an oscillation clock of said TV signal processing circuit is 14.1875MHz, a horizontal size of the image data output from said first resizing circuit is 736 pixels, and the number of horizontal pixels in the predetermined image display format is less than 736 pixels.

19. An apparatus according to Claim 16, wherein an oscillation clock of said TV signal processing circuit is 13.5MHz, a horizontal size of the image data output from said first resizing circuit is 720 pixels, and the number of horizontal pixels in the predetermined image display format is less than 720 pixels.

20. An apparatus according to Claim 16, wherein a characteristic of said LPF is changed according to a change of the predetermined image display format.

21. An apparatus according to Claim 16, wherein said LPF performs the process corresponding to image display that the number of horizontal dots in the predetermined image display format is 528 dots.

22. An apparatus according to Claim 16, wherein said LPF performs the process corresponding to image

display that the number of horizontal dots in the predetermined image display format is 220 dots.

23. An image signal processing apparatus comprising:

a first resizing circuit for resizing input image data;

a first memory for storing the image data output from said first resizing circuit;

a TV signal processing circuit for performing a predetermined signal process to the image data read from said first memory to generate a TV image signal;

a filter for performing a filtering process to the image data read from said first memory;

a data conversion circuit for converting the image data from said filter into image data of RGB data format;

a dot sequential conversion circuit for converting the RGB image data into an RGB dot sequential signal; and

a second resizing circuit for resizing the RGB dot sequential signal from said dot sequential conversion circuit.

24. An apparatus according to Claim 23, further comprising a clock generation circuit for generating a sync clock at timing of outputting the RGB dot

sequential data from said second resizing circuit.

25. An apparatus according to Claim 24, wherein said clock generation circuit generates the clock by thinning out clocks of a predetermined number from timing clocks oscillated by said TV signal processing circuit.

26. An apparatus according to Claim 23, wherein said second resizing circuit resizes the image data by a linear interpolation operation on the basis of image data of continuous two points in each color of R, G and B output by said dot sequential conversion circuit, so as to correspond to an interpolation phase at each time suitable for a resizing rate.

27. An apparatus according to Claim 23, wherein said dot sequential conversion circuit changes an RGB output dot sequential string among previously set RGB dot sequential strings, corresponding to an RGB dot sequential string of an image display unit displaying an image based on the image data output from said second resizing circuit.

28. An apparatus according to Claim 23, further comprising a second memory for temporarily storing the image data read from said first memory and being able

to asynchronously perform data writing and data reading,

wherein said filter performs the filtering process to the image data read from said second memory.

29. An apparatus according to Claim 28, further comprising a clock output circuit for outputting, as a clock for the input data of said second memory, a frequency being M/N ($M \neq N$, both are integers) of a clock oscillated to the output data of said second memory.

30. An apparatus according to Claim 23, further comprising:

an image pickup element for performing imaging of a desired subject and outputting a corresponding image signal;

an A/D (analog-to-digital) converter for converting the analog data from said image pickup element into digital data in synchronism with a clock from a first oscillator; and

an asynchronous data latch circuit for converting the digital data from said A/D converter into data synchronous with a clock from a second oscillator being asynchronous with the clock from said first oscillator.

31. An image signal processing apparatus

comprising:

a data conversion circuit for converting image data output from an image pickup element into image data of RGB data format;

a dot sequential conversion circuit for converting the image data of RGB data format output from said data conversion circuit into an RGB dot sequential signal; and

an input unit for inputting a change signal to change, in the RGB dot sequential signal output from said dot sequential conversion circuit, order of outputting R, G and B signals to an image display unit at an output destination of the RGB dot sequential signal.

32. An apparatus according to Claim 31, wherein said input unit inputs the change signal to change the order of outputting the R, G and B signals for each of an odd string and an even string of the RGB dot sequential signal.

33. An apparatus according to Claim 31, wherein said input unit inputs the change signal to change the order to any one of RGB, GBR, BRG, RBG, BGR and GRB.